REMARKS/ARGUMENTS

Claims 1-30 are pending in the present patent application. Claims 1-30 were rejected. Claims 19 and 23 have been amended. No new matter has been added to claims 19 and 23. Reconsideration of the claims is respectfully requested.

Summary of the Interview With the Examiner

Applicant would like to thank the examiner for the phone interview conducted on November 15, 2004. During the interview, the application explained the differences between the claimed invention and the cited prior art reference, U.S. Patent 5,970,005 to Yin.

The present invention relates to techniques for programming and verifying data in a programmable integrated circuit. Referring to Figure 2B of the present application, for example, address bits in row registers 621 select a first column of memory using multiplexers 652. After the first column of memory is selected, first data bits are loaded from the first column of memory to column registers 620. The same address bits in row registers 621 also select a second column of memory using multiplexers 652. After the second column of memory is selected, second data bits are loaded into the second column of memory from column registers 620.

Yin discloses loading in new address bits each time data is loaded into a memory column in programming mode and each time data is read out of a memory column for verification. See e.g., Yin at col. 11, line 36 – col. 12, line 24 and Figures 14-15.

Relative to the techniques shown in Yin, the present invention reduces the number of times the word line address bits are loaded into the row shift registers, because *one set of address bits* are used to load data into a first column of memory *and* to read data out of a second column of memory.

Claim 1, for example, recites "loading second data bits from first memory cells into the first registers, the first memory cells being in a first word line selected by first address bits in second registers; and loading the first data bits into second memory cells, the second memory cells being in a second word line selected by the first address bits."

Yin does not disclose or suggest loading second data bits from first memory cells into first registers, and loading first data bits from the first registers into second memory cells, wherein the first and second memory cells are selected by the same address bits.

According to another embodiment of the present invention, program data bits are shifted into the column shift registers *at the same time* that verify data bits are shifted out of the column shift registers. As a result, the number of times program and verify data bits are shifted into and out of the column shift registers is reduced.

Claim 25, for example, recites "shifting third data bits into the first registers while shifting the second data bits out of the first registers."

Yin does not disclose or suggest shifting programming data into the shift register at the same time that the verification data is shifted out. See e.g., Yin at col. 11, line 36 – col. 12, line 24 and Figures 14-15.

The embodiments of the present invention reduce the time delays and vector counts associated with programming and verifying data in memory cells of a PLD.

Rejections of Claims 1-30

Claims 1-30 were rejected as being obvious under 35 U.S.C. § 103 in light of U.S. Patent 5,970,005 to Yin.

Applicant respectfully submits that claims 1-30 are novel and nonobvious over the Yin patent for the reasons discussed above. Claim 19 has been amended to further clarify the scope of the claim in light of the above arguments.

Allowable Subject Matter

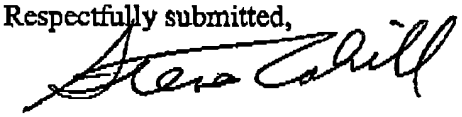
The examiner indicated that claims 16-18, 23, and 24 contain allowable subject matter. Applicant has amended claim 23 into an independent claim. Therefore, claims 23-24 are now allowable.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



Steven Cahill
Reg. No. 44,578

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 650-326-2400 Fax: 415-576-0300
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